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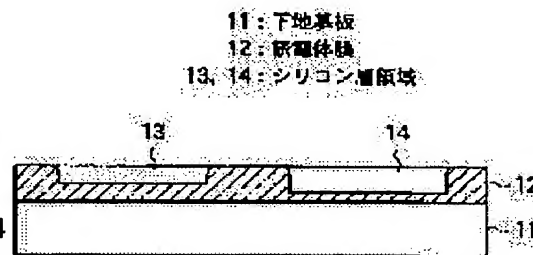
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(54) SEMICONDUCTOR SUBSTRATE, MANUFACTURING METHOD THEREOF
SEMICONDUCTOR INTEGRATED CIRCUIT

(57)Abstract:

PROBLEM TO BE SOLVED: To enable the gates of a full depletion MOS transistor and a partial depletion MOS transistor to be very accurately formed on an SOI substrate.

SOLUTION: An SOI substrate is equipped with a base substrate 11 and a dielectric film 12 laminated on the base substrate 11, and silicon layer regions 13 and 14 different from each other in thickness are formed on the dielectric film 12. The surfaces of the silicon layer regions 13 and 14 are flush with each other. Therefore, the gate electrodes of the silicon layer regions 13 and 14 can be set equal in height to each other, a resist layer to apply can be set uniform in thickness, and the gates of accurate lengths can be formed.



本発明の第1の実施形態のSOI基板

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CLAIMS

[Claim(s)]

[Claim 1] It is the semi-conductor substrate characterized by making the front face of each of this silicon layer field into the same height while said silicon layer forms two or more silicon layer fields with at least two or more kinds of different thickness in the semi-conductor substrate which has the silicon layer insulated from the substrate substrate with the dielectric film and insulating electrically between this each silicon layer field.

[Claim 2] Between said each silicon layer field, it is the semi-conductor substrate according to claim 1 characterized by insulating by being filled up with said dielectric.

[Claim 3] Said each silicon layer field is a semi-conductor substrate according to claim 1 characterized by dissociating and forming on said dielectric film.

[Claim 4] Said each silicon layer field is a semi-conductor substrate according to claim 1, 2, or 3 characterized by having the area which can form at least two or more components, respectively.

[Claim 5] The inside of the silicon layer field of two or more kinds of said thickness on a semi-conductor substrate according to claim 1, 2, 3, or 4, The circuit which used perfect depletion mold MOS transistor or this perfect depletion mold MOS transistor is formed in the thin silicon layer field of thickness. The semiconductor integrated circuit characterized by forming in the thick silicon layer field of thickness the circuit which used partial depletion mold MOS transistor or this partial depletion mold MOS transistor among the silicon layer fields of two or more kinds of said thickness.

[Claim 6] the semiconductor integrated circuit characterized by having formed in the thin silicon layer field of thickness the circuit which used MOS transistor or this MOS transistor among the silicon layer fields of two or more kinds of said thickness on a semi-conductor substrate according to claim 1, 2, 3, or 4, and forming in the thick silicon layer field of thickness the circuit which used the bipolar transistor or this bipolar transistor among the silicon layer fields of two or more kinds of said thickness.

[Claim 7] The semiconductor integrated circuit characterized by forming a passive component in said silicon layer field on a semi-conductor substrate according to claim 1, 2, 3, or 4.

[Claim 8] In the manufacture approach of a semi-conductor substrate of manufacturing a semi-conductor substrate according to claim 1, 2, or 4 By making at least 2 times or more of selective oxidation the 1st silicon substrate The process which forms in the front-face side of this 1st silicon substrate the silicon area of exposed oxide where at least three or more kinds of thickness differs, The process which carries out flattening of the front-face side of said 1st silicon substrate, and leaves and removes a part of silicon oxide in said each silicon area of exposed oxide, The manufacture approach of the semi-conductor substrate characterized by performing in order the process which removes lamination ***** and said a part of 1st silicon substrate for the 2nd silicon substrate used as said substrate substrate from a rear-face side to the front-face side of said said 1st silicon substrate by which flattening was carried out.

[Claim 9] In the manufacture approach of a semi-conductor substrate of manufacturing a semi-conductor substrate according to claim 1, 3, or 4, while forming a slot in the front-face side of the 1st silicon substrate The process which forms the silicon oxidizing zone from which at least two or more kinds of thickness differs by carrying out at least 1 times or more of selective

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oxidation, The process which leaves said some of [at least] silicon oxidation membrane layers, and carries out flattening of the front-face side of said 1st silicon substrate, The manufacture approach of the semi-conductor substrate characterized by performing in order the process which removes lamination ***** and said a part of 1st silicon substrate for the 2nd silicon substrate used as said substrate substrate from a rear-face side to the front-face side of said said 1st silicon substrate by which flattening was carried out.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the manufacture approach of the semiconductor integrated circuit formed in a semi-conductor substrate and a semi-conductor substrate, and this semi-conductor substrate.

[0002]

[Description of the Prior Art] The CMOS (Complementary Metal Oxide Semiconductor) transistor formed in the semi-conductor substrate, i.e., an SOI (Silicon On Insulator) substrate, in which the thin film silicon layer was formed on the insulating substrate or the insulator layer has a small junction capacitance between source drains, and by the reason of being able to prevent a latch rise, when advancing low-power-ization of a semiconductor integrated circuit, it attracts attention. In CMOS transistor formed on SOI structure, it is perfect depletion (Fully Depleted). A mold and partial depletion (Partially Depleted) There is a mold. A perfect depletion mold has a thin film silicon layer as thin as about 50nm or less, and the body field inserted into the source field and the drain field is always depletion-ized. In a partial depletion mold, a thin film silicon layer is comparatively as thick as 100nm or more, and the pars basilaris ossis occipitalis of a body field is not depletion-ized. Since perfect depletion mold MOS transistor can make threshold voltage low, a steep subthreshold level property being acquired and controlling OFF leakage current, it is effective in low-power-izing, but since the thin film silicon layer is as thin as about 50nm or less to coincidence, source drain resistance is high, and in order to set up substrate concentration highly, there is a fault of mobility falling and the drive capacity of a transistor declining.

[0003] On the other hand, a subthreshold level property becomes comparable as MOS transistor on a bulk substrate, and partial depletion mold MOS transistor does not have the effectiveness of low-power-izing as large as a perfect depletion mold. However, by fixing the potential of a body field, the hole produced by impact ionization working can be accumulated in a body field, and the phenomenon (kink phenomenon) of making a drain current characteristic producing distortion can be suppressed. Therefore, loading together and semiconductor-integrated-circuit-izing perfect depletion mold MOS transistor and partial depletion mold MOS transistor to the same SOI substrate in consideration of a low-power property and the stability at the time of actuation is proposed.

[0004] Drawing 2 (a) - (e) is the sectional view showing the production process of a semiconductor integrated circuit which used the conventional SOI substrate. When forming MOS transistor of a perfect depletion mold, and MOS transistor of a partial depletion mold in the same SOI substrate conventionally, the process of drawing 2 (a) - (e) is performed in order. First, SIMOX which pours in oxygen ion into a silicon single crystal substrate, and oxidizes in the process of drawing 2 (a) (Separation by IMplanted OXigen) The approach called law, Or by the approach called the lamination method shown in the following reference, the silicon oxidation membrane layer 2 is formed on a silicon substrate 1, and it is about 200nm thin film silicon layer (it is called a "SOI layer" below.) on it. The SOI substrate which has 3 is formed. Reference; JP,5-275663,A [0005] In the process of drawing 2 (b), after forming the buffer layer and silicon

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nitride layer of silicon oxide which are not illustrated on a SOI substrate and forming opening in a silicon nitride and silicon oxide through a HOTORISO process, the SOI layer 3 is alternatively oxidized by using this silicon nitride as a mask, and a silicon nitride and silicon oxide are removed. Thereby, a SOI layer forms in 70nm the field 4 which became thin. In the process of drawing 2 (c), the SOI layer 3 is etched alternatively, and while forming the field 6 which forms partial depletion mold MOS transistor in locations other than field 4, the field 5 which forms perfect depletion mold MOS transistor in a location including a field 4 is formed. It is the process of this drawing 2 (c), next CMOS transistor is formed. In addition, although drawing 2 (d) and (e) explain the case where N channel mold MOS transistor (henceforth "NMOS") is formed, also when forming P channel mold MOS transistor (henceforth "PMOS"), it can form at the same process only by replacing the type of an impurity with.

[0006] In the process of drawing 2 (d), the P type impurity for controlling the threshold voltage of MOS transistor is poured in, the laminating of the gate oxide 7 is carried out on the SOI layer 3 of fields 5 and 6, and the polish recon 8 used as a gate electrode is formed on it. Furthermore, it is P+ to the part which injects a high concentration P type impurity into a part of SOI layer 3, and serves as the source of partial depletion mold MOS transistor. A field 9 is generated. N+ which pours an N type impurity into high concentration, and becomes the source and a drain in the process of drawing 2 (e) A field 10 is formed in the SOI layer 3. At this time, it is P+. The part which does not pour in and pour an N type impurity into a part of field 9 is P+. P+ which became as [impurity range] and poured in the N type impurity The pars basilaris ossis occipitalis of a field 9 becomes a P type impurity range. Of the above, perfect depletion mold MOS transistor and partial depletion mold MOS transistor are formed. After carrying out the laminating of the interlayer insulation film to the substrate with which this MOS transistor was formed, opening of the contact hole is carried out to the source, a drain, the gate, and a body contact field, metal wiring is formed, and a semiconductor integrated circuit is manufactured.

[0007]

[Problem(s) to be Solved by the Invention] However, by the manufacture approach which forms a semiconductor integrated circuit, the following technical problems were in the conventional SOI substrate. Since the field 4 which forms the gate electrode of perfect depletion mold MOS transistor had become a concave, in order to form the polish recon 8 used as a gate electrode, when applying the resist film, this resist thickness became thicker than the circumference, and control of a gate length dimension tended to become difficult, and problems, like a gate electrode is narrow in the case of etching were produced, and there were things. Furthermore, since the height of the gate electrode of perfect depletion mold MOS transistor and partial depletion mold MOS transistor differed, it was difficult to double the gate length dimension of both transistors.

[0008]

[Means for Solving the Problem] In order to solve said technical problem, 1st invention is carried out to the following configurations in the SOI substrate which has the silicon layer insulated from the substrate substrate with the dielectric film. That is, said silicon layer forms two or more silicon layer fields with at least two or more kinds of different thickness, and between this each silicon layer field, the front face of each of this silicon layer field is made into the same height while insulating electrically. The 2nd invention has insulated by being filled up with said dielectric between said each silicon layer field in the SOI substrate of the 1st invention. In the SOI substrate of the 1st invention, it dissociates on said dielectric film and the 3rd invention forms said each silicon layer field. In the 1st, the 2nd, or the SOI substrate of the 3rd invention, said each silicon layer field is carrying out 4th invention to the configuration which has the area which can form at least two or more components, respectively.

[0009] Set the 5th invention to a semiconductor integrated circuit, and in the thin silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness on the 1-3rd or the SOI substrate of the 4th invention The circuit using perfect depletion mold MOS transistor or this perfect depletion mold MOS transistor is formed. In the thick silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness The circuit using partial depletion mold MOS transistor or this partial depletion mold MOS transistor is formed. Set the 6th invention to a semiconductor integrated circuit, and in the thin silicon layer

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field of the thickness of the silicon layer fields of two or more kinds of said thickness on the 1-3rd or the SOI substrate of the 4th invention The circuit using MOS transistor or this MOS transistor is formed, and the circuit which used the bipolar transistor or this bipolar transistor is formed in the thick silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness.

[0010] In a semiconductor integrated circuit, the 7th invention can be set on the 1-3rd or the SOI substrate of the 4th invention, and forms the passive component in a silicon layer field. The 8th invention has devised the following approaches in the manufacture approach of a semiconductor substrate of manufacturing the 1st, 2, or the semi-conductor substrate of the 4th invention. Namely, by making at least 2 times or more of selective oxidation the 1st silicon substrate The process which forms in the front-face side of this 1st silicon substrate at least three or more kinds of silicon area of exposed oxides where thickness differs, The process which carries out flattening of the front-face side of said 1st silicon substrate, and leaves and removes a part of silicon oxide in said each silicon area of exposed oxide, It is made to perform in order the process which removes lamination ***** and said a part of 1st silicon substrate for the 2nd silicon substrate used as said substrate substrate from a rear-face side to the front-face side of said said 1st silicon substrate by which flattening was carried out.

[0011] In the manufacture approach of a semi-conductor substrate of manufacturing a semi-conductor substrate according to claim 1, 3, or 4, while the 9th invention forms a slot in the front-face side of the 1st silicon substrate The process which forms at least two or more kinds of silicon oxidizing zones from which thickness differs by carrying out at least 1 times or more of selective oxidation, The process which leaves said some of [at least] silicon oxidation membrane layers, and carries out flattening of the front-face side of said 1st silicon substrate, It is made to perform in order the process which removes lamination ***** and said a part of 1st silicon substrate for the 2nd silicon substrate used as said substrate substrate from a rear-face side to the front-face side of said said 1st silicon substrate by which flattening was carried out.

[0012] According to the 1st to 9th invention, since the manufacture approach of a SOI substrate, a semiconductor integrated circuit, and a SOI substrate was constituted as mentioned above, the silicon layer field where thickness differs is formed on a dielectric film, and the height of the front face of those silicon layer fields is the same. Therefore, the height of the gate electrode of MOS transistor formed on the silicon field of a SOI substrate will gather. According to the 4th invention, moreover, each silicon layer field Since it has the area which can form at least two or more components, respectively, for example to the thin silicon layer field of thickness A circuit with rapidity and low-power nature and the circuit where stability is searched for are loaded together by the common substrate by forming the circuit using perfect depletion mold MOS transistor, and forming the circuit which used partial depletion mold MOS transistor for the thick silicon layer field of thickness.

[0013]
 [Embodiment of the Invention] The 1st operation gestalt drawing 1 is the sectional view of the SOI substrate in which the 1st operation gestalt of this invention is shown. This SOI substrate has the dielectric film 12 by which the laminating was carried out on the substrate substrate 11 and this substrate substrate 11, and the silicon layer fields 13 and 14 of two kinds of different thickness are formed on this dielectric film 12. between the silicon layer fields 13 and 14 -- a dielectric film 12 -- **** -- while dissociating electrically, the surface height of these silicon layer fields 13 and 14 is the same.

[0014] Drawing 3 (a) - (e) is the sectional view showing the production process of the SOI substrate of drawing 1 . Drawing 4 (a) - (c) is the sectional view showing the production process of a semiconductor integrated circuit which used the SOI substrate of drawing 1 . In order to form the SOI substrate of drawing 1 , the process of drawing 3 (a) - (e) is performed in order. The process of the first drawing 3 (a) is a process which forms the 1st silicon substrate 20 of a three-tiered structure, and after it forms the porosity silicon layer 22 with a thickness of about 20 micrometers in the front face of the P type silicon substrate 21 and oxidizes, it carries out EPITAKYARU growth of the single-crystal-silicon layer 23 of about 200nm thickness by the CVD (Chemical Vapor Deposition) method.

[0015] At the process of next drawing 3 (b) of drawing 3 (a), while carrying out the laminating of

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the silicon oxidation membrane layer 24 used as a buffer layer to the front face of the single-crystal-silicon layer 23, after forming the silicon nitride layer 25, opening of this a part of silicon nitride layer 25 26 is carried out according to a HOTORISO process. And selective oxidation is performed and thickness of the silicon oxide in a part 26 is made into the thickness of about 50nm. In the process of drawing 3 (c), a HOTORISO process is performed to the part 27 of the fields where the silicon nitride layer 25 remains, this silicon nitride layer 25 removes, selective oxidation is performed, and thickness of silicon oxide [in / both / a part 27] which grows up the thickness of the silicon oxide in a part 26 into about 200nm is set to about 150nm.

[0016] After removing the silicon nitride layer 25 which remained in the process of drawing 3 (d), the single-crystal-silicon layer 23 forms the silicon area of exposed oxide 28 which oxidized altogether, the silicon area of exposed oxide 29 which left about 50nm of single-crystal-silicon layers 23, and oxidized, and the silicon area of exposed oxide 30 which left about 100nm of single-crystal-silicon layers 23, and oxidized by performing thermal oxidation.

[0017] In the process of drawing 3 (e), the front face where the substrate of drawing 3 (d) oxidized is evenly ground by a chemical mechanical-polishing method etc. Superposition and heat treatment are performed so that this polished surface may touch the 2nd silicon substrate 31 prepared separately in the substrate with which the front face was ground, and it is ***** firmly. The silicon substrate 31 side of the ***** (ed) substrate is covered with a silicon nitride, using the mixed liquor of a nitric acid and fluoric acid, it leaves the porosity silicon layer 22 by the side of a substrate 20, and etching removal is carried out. Furthermore, the porosity silicon layer 22 is also removed using the mixed liquor of a nitric acid, fluoric acid, and an acetic acid. The single-crystal-silicon layer 23 is not removed by these etching. Therefore, the SOI layers 32 and 33 separated electrically [this substrate 31] in the silicon area of exposed oxides 29 and 30 are formed on a substrate 31. It dissociates electrically between the SOI layers 32 and 33 in the silicon area of exposed oxide 28. That is, the SOI substrate of drawing 1 is formed. A substrate 31 turns into the substrate substrate 11, the silicon area of exposed oxides 28, 29, and 30 serve as a dielectric layer 12, and the SOI layers 32 and 33 serve as the silicon layer fields 13 and 14 where thickness differs.

[0018] In manufacturing the semiconductor integrated circuit which has a CMOS transistor, using the SOI substrate of drawing 1 , it performs the process of drawing 4 (a) - (c) in order. In addition, although drawing 4 (a) - (c) explains the case where NMOS are formed, also when forming PMOS, it can form at the same process only by replacing the type of an impurity with. First, in the process of drawing 4 (a), in order to control the threshold voltage of MOS transistor, after pouring in a P type impurity, carrying out the laminating of the gate oxide 34 to the front face of the SOI layers 32 and 33 which constitute the silicon layer fields 13 and 14, and the exposed dielectric film 12 and applying a resist on this gate oxide 34, a resist pattern is formed by the electron-beam-exposure method. And dry etching which used the resist pattern as the mask is performed, and the gate electrode 35 is formed.

[0019] In the process of drawing 4 (b), silicon oxide is formed all over the main front face, anisotropic etching is performed and a sidewall 36 is formed in the side attachment wall of the gate electrode 35. An N type impurity is poured into the source field and drain field of MOS transistor in the process of drawing 4 (c), and it is N+. After forming a layer 37, the main front face of a substrate is made to carry out selective growth of the W (tungsten) film 38 with a CVD method. Furthermore, after depositing an interlayer insulation film on the main front face of a substrate in which the W film 38 was formed, opening of the contact hole is carried out to the source, a drain, the gate, and a body contact field, and metal wiring is performed. MOS transistor which MOS transistor of a semiconductor integrated circuit was formed of a series of processes of above drawing 4 (a) - (c), and was formed on the thin SOI layer 32 of thickness of them turns into perfect depletion mold MOS transistor, and MOS transistor formed on the thick SOI layer 33 of thickness turns into partial depletion mold MOS transistor. Here, it is formed in a body field without the gate electrode 35 in a space near side of partial depletion mold MOS transistor formed on the thick SOI layer 32 of thickness although the body contact field is not illustrated. That is, it means that perfect depletion mold MOS transistor and partial depletion mold MOS transistor which has contact to a body field had been loaded together by the semiconductor

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integrated circuit.

[0020] As mentioned above, while the thick SOI layer 33 of the thickness suitable for forming the thin SOI layer 32 of the thickness which was suitable for forming perfect depletion mold MOS transistor with this 1st operation gestalt with the production process of drawing 3 (a) – (e), and partial depletion mold MOS transistor is separated by the dielectric film 12, the SOI substrate with which that surface height became flat is formed. Therefore, if a semiconductor integrated circuit is manufactured using a SOI substrate, a set and the resist thickness to apply become fixed and the height of the polish recon of perfect depletion mold MOS transistor and partial depletion mold MOS transistor can form the die length of the gate electrode 35 in homogeneity with a sufficient precision. Therefore, formation of a good semiconductor integrated circuit without the vena contracta of a pattern etc. is attained. Since perfect depletion mold MOS transistor and partial depletion mold MOS transistor can moreover be formed at the almost same process on the same substrate, while excelling in low cost-ization, productivity improves. Furthermore, since the thickness of the SOI layers 31 and 32 is decided by an epitaxial growth process, an oxidation process, etc. of single crystal silicon, the homogeneity is excellent while control of thickness is easy.

[0021] The 2nd operation gestalt drawing 5 is the sectional view of the SOI substrate in which the 2nd operation gestalt of this invention is shown. This SOI substrate is a substrate which has the silicon layer insulated from the substrate substrate 41 with the dielectric film 42, this silicon layer forms the silicon layer fields 43 and 44 with at least two or more kinds of different thickness, and while insulating electrically between this each silicon layer field 43 and 44 in a slot, the front face of each of these silicon fields 43 and 44 has the same height.

[0022] Drawing 6 (a) – (d) is the sectional view showing the production process of the SOI substrate of drawing 5, and it explains the manufacture approach of the SOI substrate of drawing 5, referring to this drawing 6 (a) – (d). First, the process of drawing 6 (a) is a process which forms the 1st silicon substrate 50 of a three-tiered structure, and after it forms the porosity silicon layer 52 with a thickness of about 10 micrometers in the front face of the P type silicon substrate 51 and oxidizes, it carries out EPITAKYARU growth of the single-crystal-silicon layer 53 of about 200nm thickness with a CVD method.

[0023] At the process of next drawing 6 (b) of drawing 6 (a), therefore, silicon oxide 54 is formed in thermal oxidation on the single-crystal-silicon layer 53, and the silicon nitride 55 is further formed on this silicon oxide 54. Then, opening of the silicon nitride 55 and the silicon oxide 54 is carried out partially, according to a HOTORISO process, the single-crystal-silicon layer 53 is etched until it reaches the porosity silicon layer 52, and the structure which divided the single-crystal-silicon layer 53 in the slot 56 is formed. In the process of drawing 6 (c), after a HOTORISO process removes the silicon nitride 55 partially, the silicon area of exposed oxide 57 of about 300nm thickness is formed by selective oxidation.

[0024] In the process of drawing 6 (d), by a chemical mechanical-polishing method etc., it grinds and flattening of the front face is carried out until the silicon nitride 55 is lost. At this time, a part of silicon area of exposed oxide 57 remains, without being ground. Superposition and heat treatment are performed so that this polished surface may touch the 2nd silicon substrate 41 prepared separately in the substrate with which the front face was ground, and it is ***** firmly. The silicon substrate 41 side of the ***** (ed) substrate is covered with a silicon nitride, using the mixed liquor of a nitric acid and fluoric acid, it leaves the porosity silicon layer 52 by the side of a substrate 50, and etching removal is carried out. Furthermore, the porosity silicon layer 52 is also removed using the mixed liquor of a nitric acid, fluoric acid, and an acetic acid. The single-crystal-silicon layer 53 is not removed by these etching. Therefore, the SOI layers 58 and 59 separated electrically [this substrate 41] at silicon oxide 54 and 57 are formed on a substrate 41. Among the SOI layers 58 and 59, there is a slot 56 and it dissociates electrically. That is, the SOI substrate of drawing 5 is formed. Silicon oxide 54 and 57 serves as a dielectric layer 42, and the SOI layers 58 and 59 serve as the silicon layer fields 43 and 44 where thickness differs.

[0025] As mentioned above, while dissociating by the thick SOI layer 59 and thick fang furrow 56 of thickness suitable for forming the thin SOI layer 58 of the thickness which was suitable for

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forming perfect depletion mold MOS transistor with this 2nd operation gestalt with drawing 6 (a) – (d), and partial depletion mold MOS transistor, the SOI substrate with which that surface height became flat is formed. Therefore, like the 1st operation gestalt, if a semiconductor integrated circuit is manufactured using a SOI substrate, a set and the resist thickness to apply become fixed and the height of the polish recon of perfect depletion mold MOS transistor and partial depletion mold MOS transistor can form the die length of the gate electrode 35 in homogeneity with a sufficient precision. Therefore, formation of a good semiconductor integrated circuit without the vena contracta of a pattern etc. is attained.

[0026] The 3rd operation gestalt drawing 7 is the top view of the SOI substrate in which the 3rd operation gestalt of this invention is shown, and the common sign is given to the element in drawing 1 which shows the 1st operation gestalt, and the common element. It is the substrate manufactured according to the same process as the 1st operation gestalt, and this SOI substrate has the silicon layer field 13 formed in the SOI layer whose thickness is about 50nm, and the silicon layer field 14 formed in the SOI layer whose thickness is about 100nm. It is separated between the silicon layer field 13 and the silicon layer field 14 by the dielectric film 12 formed by the silicon oxidation membrane layer. The silicon layer field 13 and the silicon layer field 14 have the area which can form two or more MOS transistors, respectively, respectively. The digital circuit group which used perfect depletion mold MOS transistor is formed in the thin silicon layer field 13 of thickness, and the analog circuit group which used partial depletion mold MOS transistor is formed in the thick silicon layer field 14 of thickness. By doing in this way, it is possible to load together an analog circuit group and a digital circuit group to a common substrate.

[0027] As mentioned above, with this 3rd operation gestalt, the silicon layer field 13 and the silicon layer field 14 are a SOI substrate with the area which can form two or more MOS transistors, respectively, and mixed loading of an analog circuit group and a digital circuit group is attained. Therefore, an analog circuit group with the high stability at the time of the actuation using the digital circuit group excellent in the rapidity and low-power nature using perfect depletion mold MOS transistor and partial depletion mold MOS transistor which has body contact can be manufactured now to coincidence at the same process. Therefore, the analog digital mixed-loading circuit of high performance can be manufactured by low cost, and productivity is high. Furthermore, since the digital circuit group and the analog circuit group are separated by the dielectric film 12, it can prevent that the noise generated by the digital circuit group arrives at the field of an analog circuit group, and degrades the property of this analog circuit group. If the substrate which formed in the predetermined location beforehand the fields 13 and 14 where the thickness of a SOI layer differs about the product with the respectively almost comparable scale of a digital circuit group and an analog circuit group is moreover created, the period from a circuit design to manufacture can be shortened sharply.

[0028] In addition, this invention is not limited to the above-mentioned operation gestalt, but various deformation is possible for it. As the modification, there is the following, for example.

(1) Although it was made the configuration which forms perfect depletion mold MOS transistor in the thin SOI layers 32 and 58 of thickness, and forms ***** type MOS transistor in the thick SOI layers 33 and 59 of thickness, a bipolar transistor is formed in the thick SOI layers 33 and 59 of this thickness, and you may make it, manufacture the semiconductor integrated circuit consolidated with MOS transistor and a bipolar transistor for example.

(2) In the SOI layers 32, 33, 58, and 59, not only a transistor but passive components, such as in TAKUTA and a capacitor, may be formed and semiconductor-integrated-circuit-ized.

[0029]

[Effect of the Invention] According to the 1st – the 9th invention, as explained to the detail above, the silicon layer field where thickness differs is formed on a dielectric film, and since the height of the front face of those silicon layer fields is the same The height of the gate electrode of MOS transistor formed on this silicon layer field will gather, the die length of this gate electrode can form with a sufficient precision, and formation of a good semiconductor integrated circuit without the vena contracta of a pattern etc. is attained. Since perfect depletion mold MOS transistor and partial depletion mold MOS transistor can moreover be formed at the almost

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same process on the same substrate, while excelling in low cost-ization, productivity improves. [0030] Moreover, according to the 4th invention, each silicon layer field Since it has the area which can form at least two or more components, respectively, for example to the thin silicon layer field of thickness A digital circuit with rapidity and low-power nature and the analog circuit where stability is searched for are made in mixed loading at a common substrate by forming the circuit using perfect depletion mold MOS transistor, and forming the circuit which used partial depletion mold MOS transistor for the thick silicon layer field of thickness.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, by the manufacture approach which forms a semiconductor integrated circuit, the following technical problems were in the conventional SOI substrate. Since the field 4 which forms the gate electrode of perfect depletion mold MOS transistor had become a concave, in order to form the polish recon 8 used as a gate electrode, when applying the resist film, this resist thickness became thicker than the circumference, and control of a gate length dimension tended to become difficult, and problems, like a gate electrode is narrow in the case of etching were produced, and there were things. Furthermore, since the height of the gate electrode of perfect depletion mold MOS transistor and partial depletion mold MOS transistor differed, it was difficult to double the gate length dimension of both transistors.

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MEANS

[Means for Solving the Problem] In order to solve said technical problem, 1st invention is carried out to the following configurations in the SOI substrate which has the silicon layer insulated from the substrate with the dielectric film. That is, said silicon layer forms two or more silicon layer fields with at least two or more kinds of different thickness, and between this each silicon layer field, the front face of each of this silicon layer field is made into the same height while insulating electrically. The 2nd invention has insulated by being filled up with said dielectric between said each silicon layer field in the SOI substrate of the 1st invention. In the SOI substrate of the 1st invention, it dissociates on said dielectric film and the 3rd invention forms said each silicon layer field. In the 1st, the 2nd, or the SOI substrate of the 3rd invention, said each silicon layer field is carrying out 4th invention to the configuration which has the area which can form at least two or more components, respectively.

[0009] Set the 5th invention to a semiconductor integrated circuit, and in the thin silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness on the 1-3rd or the SOI substrate of the 4th invention The circuit using perfect depletion mold MOS transistor or this perfect depletion mold MOS transistor is formed. In the thick silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness The circuit using partial depletion mold MOS transistor or this partial depletion mold MOS transistor is formed. Set the 6th invention to a semiconductor integrated circuit, and in the thin silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness on the 1-3rd or the SOI substrate of the 4th invention The circuit using MOS transistor or this MOS transistor is formed, and the circuit which used the bipolar transistor or this bipolar transistor is formed in the thick silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness.

[0010] In a semiconductor integrated circuit, the 7th invention can be set on the 1-3rd or the SOI substrate of the 4th invention, and forms the passive component in a silicon layer field. The 8th invention has devised the following approaches in the manufacture approach of a semiconductor substrate of manufacturing the 1st, 2, or the semi-conductor substrate of the 4th invention. Namely, by making at least 2 times or more of selective oxidation the 1st silicon substrate The process which forms in the front-face side of this 1st silicon substrate at least three or more kinds of silicon area of exposed oxides where thickness differs, The process which carries out flattening of the front-face side of said 1st silicon substrate, and leaves and removes a part of silicon oxide in said each silicon area of exposed oxide, It is made to perform in order the process which removes lamination ***** and said a part of 1st silicon substrate for the 2nd silicon substrate used as said substrate substrate from a rear-face side to the front-face side of said said 1st silicon substrate by which flattening was carried out.

[0011] In the manufacture approach of a semi-conductor substrate of manufacturing a semi-conductor substrate according to claim 1, 3, or 4, while the 9th invention forms a slot in the front-face side of the 1st silicon substrate The process which forms at least two or more kinds of silicon oxidizing zones from which thickness differs by carrying out at least 1 times or more of selective oxidation, The process which leaves said some of [at least] silicon oxidation membrane layers, and carries out flattening of the front-face side of said 1st silicon substrate, It

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is made to perform in order the process which removes lamination ***** and said a part of 1st silicon substrate for the 2nd silicon substrate used as said substrate substrate from a rear-face side to the front-face side of said said 1st silicon substrate by which flattening was carried out. [0012] According to the 1st to 9th invention, since the manufacture approach of a SOI substrate, a semiconductor integrated circuit, and a SOI substrate was constituted as mentioned above, the silicon layer field where thickness differs is formed on a dielectric film, and the height of the front face of those silicon layer fields is the same. Therefore, the height of the gate electrode of MOS transistor formed on the silicon field of a SOI substrate will gather. According to the 4th invention, moreover, each silicon layer field Since it has the area which can form at least two or more components, respectively, for example to the thin silicon layer field of thickness A circuit with rapidity and low-power nature and the circuit where stability is searched for are loaded together by the common substrate by forming the circuit using perfect depletion mold MOS transistor, and forming the circuit which used partial depletion mold MOS transistor for the thick silicon layer field of thickness.

[0013]

[Embodiment of the Invention] The 1st operation gestalt drawing 1 is the sectional view of the SOI substrate in which the 1st operation gestalt of this invention is shown. This SOI substrate has the dielectric film 12 by which the laminating was carried out on the substrate substrate 11 and this substrate substrate 11, and the silicon layer fields 13 and 14 of two kinds of different thickness are formed on this dielectric film 12. between the silicon layer fields 13 and 14 -- a dielectric film 12 -- **** -- while dissociating electrically, the surface height of these silicon layer fields 13 and 14 is the same.

[0014] Drawing 3 (a) - (e) is the sectional view showing the production process of the SOI substrate of drawing 1. Drawing 4 (a) - (c) is the sectional view showing the production process of a semiconductor integrated circuit which used the SOI substrate of drawing 1. In order to form the SOI substrate of drawing 1, the process of drawing 3 (a) - (e) is performed in order. The process of the first drawing 3 (a) is a process which forms the 1st silicon substrate 20 of a three-tiered structure, and after it forms the porosity silicon layer 22 with a thickness of about 20 micrometers in the front face of the P type silicon substrate 21 and oxidizes, it carries out EPITAKYARU growth of the single-crystal-silicon layer 23 of about 200nm thickness by the CVD (Chemical Vapor Deposition) method.

[0015] At the process of next drawing 3 (b) of drawing 3 (a), while carrying out the laminating of the silicon oxidation membrane layer 24 used as a buffer layer to the front face of the single-crystal-silicon layer 23, after forming the silicon nitride layer 25, opening of this a part of silicon nitride layer 25 26 is carried out according to a HOTORISO process. And selective oxidation is performed and thickness of the silicon oxide in a part 26 is made into the thickness of about 50nm. In the process of drawing 3 (c), a HOTORISO process is performed to the part 27 of the fields where the silicon nitride layer 25 remains, this silicon nitride layer 25 removes, selective oxidation is performed, and thickness of silicon oxide [in / both / a part 27] which grows up the thickness of the silicon oxide in a part 26 into about 200nm is set to about 150nm.

[0016] After removing the silicon nitride layer 25 which remained in the process of drawing 3 (d), the single-crystal-silicon layer 23 forms the silicon area of exposed oxide 28 which oxidized altogether, the silicon area of exposed oxide 29 which left about 50nm of single-crystal-silicon layers 23, and oxidized, and the silicon area of exposed oxide 30 which left about 100nm of single-crystal-silicon layers 23, and oxidized by performing thermal oxidation.

[0017] In the process of drawing 3 (e), the front face where the substrate of drawing 3 (d) oxidized is evenly ground by a chemical mechanical-polishing method etc. Superposition and heat treatment are performed so that this polished surface may touch the 2nd silicon substrate 31 prepared separately in the substrate with which the front face was ground, and it is ***** firmly. The silicon substrate 31 side of the ***** (ed) substrate is covered with a silicon nitride, using the mixed liquor of a nitric acid and fluoric acid, it leaves the porosity silicon layer 22 by the side of a substrate 20, and etching removal is carried out. Furthermore, the porosity silicon layer 22 is also removed using the mixed liquor of a nitric acid, fluoric acid, and an acetic acid. The single-crystal-silicon layer 23 is not removed by these etching. Therefore, the SOI layers 32

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and 33 separated electrically [this substrate 31] in the silicon area of exposed oxides 29 and 30 are formed on a substrate 31. It dissociates electrically between the SOI layers 32 and 33 in the silicon area of exposed oxide 28. That is, the SOI substrate of drawing 1 is formed. A substrate 31 turns into the substrate substrate 11, the silicon area of exposed oxides 28, 29, and 30 serve as a dielectric layer 12, and the SOI layers 32 and 33 serve as the silicon layer fields 13 and 14 where thickness differs.

[0018] In manufacturing the semiconductor integrated circuit which has a CMOS transistor, using the SOI substrate of drawing 1 , it performs the process of drawing 4 (a) – (c) in order. In addition, although drawing 4 (a) – (c) explains the case where NMOS are formed, also when forming PMOS, it can form at the same process only by replacing the type of an impurity with. First, in the process of drawing 4 (a), in order to control the threshold voltage of MOS transistor, after pouring in a P type impurity, carrying out the laminating of the gate oxide 34 to the front face of the SOI layers 32 and 33 which constitute the silicon layer fields 13 and 14, and the exposed dielectric film 12 and applying a resist on this gate oxide 34, a resist pattern is formed by the electron-beam-exposure method. And dry etching which used the resist pattern as the mask is performed, and the gate electrode 35 is formed.

[0019] In the process of drawing 4 (b), silicon oxide is formed all over the main front face, anisotropic etching is performed and a sidewall 36 is formed in the side attachment wall of the gate electrode 35. An N type impurity is poured into the source field and drain field of MOS transistor in the process of drawing 4 (c), and it is N+. After forming a layer 37, the main front face of a substrate is made to carry out selective growth of the W (tungsten) film 38 with a CVD method. Furthermore, after depositing an interlayer insulation film on the main front face of a substrate in which the W film 38 was formed, opening of the contact hole is carried out to the source, a drain, the gate, and a body contact field, and metal wiring is performed. MOS transistor which MOS transistor of a semiconductor integrated circuit was formed of a series of processes of above drawing 4 (a) – (c), and was formed on the thin SOI layer 32 of thickness of them turns into perfect depletion mold MOS transistor, and MOS transistor formed on the thick SOI layer 33 of thickness turns into partial depletion mold MOS transistor. Here, it is formed in a body field without the gate electrode 35 in a space near side of partial depletion mold MOS transistor formed on the thick SOI layer 32 of thickness although the body contact field is not illustrated. That is, it means that perfect depletion mold MOS transistor and partial depletion mold MOS transistor which has contact to a body field had been loaded together by the semiconductor integrated circuit.

[0020] As mentioned above, while the thick SOI layer 33 of the thickness suitable for forming the thin SOI layer 32 of the thickness which was suitable for forming perfect depletion mold MOS transistor with this 1st operation gestalt with the production process of drawing 3 (a) – (e), and partial depletion mold MOS transistor is separated by the dielectric film 12, the SOI substrate with which that surface height became flat is formed. Therefore, if a semiconductor integrated circuit is manufactured using a SOI substrate, a set and the resist thickness to apply become fixed and the height of the polish recon of perfect depletion mold MOS transistor and partial depletion mold MOS transistor can form the die length of the gate electrode 35 in homogeneity with a sufficient precision. Therefore, formation of a good semiconductor integrated circuit without the vena contracta of a pattern etc. is attained. Since perfect depletion mold MOS transistor and partial depletion mold MOS transistor can moreover be formed at the almost same process on the same substrate, while excelling in low cost-ization, productivity improves. Furthermore, since the thickness of the SOI layers 31 and 32 is decided by an epitaxial growth process, an oxidation process, etc. of single crystal silicon, the homogeneity is excellent while control of thickness is easy.

[0021] The 2nd operation gestalt drawing 5 is the sectional view of the SOI substrate in which the 2nd operation gestalt of this invention is shown. This SOI substrate is a substrate which has the silicon layer insulated from the substrate substrate 41 with the dielectric film 42, this silicon layer forms the silicon layer fields 43 and 44 with at least two or more kinds of different thickness, and while insulating electrically between this each silicon layer field 43 and 44 in a slot, the front face of each of these silicon fields 43 and 44 has the same height.

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[0022] Drawing 6 (a) – (d) is the sectional view showing the production process of the SOI substrate of drawing 5, and it explains the manufacture approach of the SOI substrate of drawing 5, referring to this drawing 6 (a) – (d). First, the process of drawing 6 (a) is a process which forms the 1st silicon substrate 50 of a three-tiered structure, and after it forms the porosity silicon layer 52 with a thickness of about 10 micrometers in the front face of the P type silicon substrate 51 and oxidizes, it carries out EPITAXY growth of the single-crystal-silicon layer 53 of about 200nm thickness with a CVD method.

[0023] At the process of next drawing 6 (b) of drawing 6 (a), therefore, silicon oxide 54 is formed in thermal oxidation on the single-crystal-silicon layer 53, and the silicon nitride 55 is further formed on this silicon oxide 54. Then, opening of the silicon nitride 55 and the silicon oxide 54 is carried out partially, according to a HOTORISO process, the single-crystal-silicon layer 53 is etched until it reaches the porosity silicon layer 52, and the structure which divided the single-crystal-silicon layer 53 in the slot 56 is formed. In the process of drawing 6 (c), after a HOTORISO process removes the silicon nitride 55 partially, the silicon area of exposed oxide 57 of about 300nm thickness is formed by selective oxidation.

[0024] In the process of drawing 6 (d), by a chemical mechanical-polishing method etc., it grinds and flattening of the front face is carried out until the silicon nitride 55 is lost. At this time, a part of silicon area of exposed oxide 57 remains, without being ground. Superposition and heat treatment are performed so that this polished surface may touch the 2nd silicon substrate 41 prepared separately in the substrate with which the front face was ground, and it is ***** firmly. The silicon substrate 41 side of the ***** (ed) substrate is covered with a silicon nitride, using the mixed liquor of a nitric acid and fluoric acid, it leaves the porosity silicon layer 52 by the side of a substrate 50, and etching removal is carried out. Furthermore, the porosity silicon layer 52 is also removed using the mixed liquor of a nitric acid, fluoric acid, and an acetic acid. The single-crystal-silicon layer 53 is not removed by these etching. Therefore, the SOI layers 58 and 59 separated electrically [this substrate 41] at silicon oxide 54 and 57 are formed on a substrate 41. Among the SOI layers 58 and 59, there is a slot 56 and it dissociates electrically. That is, the SOI substrate of drawing 5 is formed. Silicon oxide 54 and 57 serves as a dielectric layer 42, and the SOI layers 58 and 59 serve as the silicon layer fields 43 and 44 where thickness differs.

[0025] As mentioned above, while dissociating by the thick SOI layer 59 and thick fang furrow 56 of thickness suitable for forming the thin SOI layer 58 of the thickness which was suitable for forming perfect depletion mold MOS transistor with this 2nd operation gestalt with drawing 6 (a) – (d), and partial depletion mold MOS transistor, the SOI substrate with which that surface height became flat is formed. Therefore, like the 1st operation gestalt, if a semiconductor integrated circuit is manufactured using a SOI substrate, a set and the resist thickness to apply become fixed and the height of the polish recon of perfect depletion mold MOS transistor and partial depletion mold MOS transistor can form the die length of the gate electrode 35 in homogeneity with a sufficient precision. Therefore, formation of a good semiconductor integrated circuit without the vena contracta of a pattern etc. is attained.

[0026] The 3rd operation gestalt drawing 7 is the top view of the SOI substrate in which the 3rd operation gestalt of this invention is shown, and the common sign is given to the element in drawing 1 which shows the 1st operation gestalt, and the common element. It is the substrate manufactured according to the same process as the 1st operation gestalt, and this SOI substrate has the silicon layer field 13 formed in the SOI layer whose thickness is about 50nm, and the silicon layer field 14 formed in the SOI layer whose thickness is about 100nm. It is separated between the silicon layer field 13 and the silicon layer field 14 by the dielectric film 12 formed by the silicon oxidation membrane layer. The silicon layer field 13 and the silicon layer field 14 have the area which can form two or more MOS transistors, respectively, respectively. The digital circuit group which used perfect depletion mold MOS transistor is formed in the thin silicon layer field 13 of thickness, and the analog circuit group which used partial depletion mold MOS transistor is formed in the thick silicon layer field 14 of thickness. By doing in this way, it is possible to load together an analog circuit group and a digital circuit group to a common substrate.

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[0027] As mentioned above, with this 3rd operation gestalt, the silicon layer field 13 and the silicon layer field 14 are a SOI substrate with the area which can form two or more MOS transistors, respectively, and mixed loading of an analog circuit group and a digital circuit group is attained. Therefore, an analog circuit group with the high stability at the time of the actuation using the digital circuit group excellent in the rapidity and low-power nature using perfect depletion mold MOS transistor and partial depletion mold MOS transistor which has body contact can be manufactured now to coincidence at the same process. Therefore, the analog digital mixed-loading circuit of high performance can be manufactured by low cost, and productivity is high. Furthermore, since the digital circuit group and the analog circuit group are separated by the dielectric film 12, it can prevent that the noise generated by the digital circuit group arrives at the field of an analog circuit group, and degrades the property of this analog circuit group. If the substrate which formed in the predetermined location beforehand the fields 13 and 14 where the thickness of a SOI layer differs about the product with the respectively almost comparable scale of a digital circuit group and an analog circuit group is moreover created, the period from a circuit design to manufacture can be shortened sharply.

[0028] In addition, this invention is not limited to the above-mentioned operation gestalt, but various deformation is possible for it. As the modification, there is the following, for example.

(1) Although it was made the configuration which forms perfect depletion mold MOS transistor in the thin SOI layers 32 and 58 of thickness, and forms ***** type MOS transistor in the thick SOI layers 33 and 59 of thickness, a bipolar transistor is formed in the thick SOI layers 33 and 59 of this thickness, and you may make it, manufacture the semiconductor integrated circuit consolidated with MOS transistor and a bipolar transistor for example.

(2) In the SOI layers 32, 33, 58, and 59, not only a transistor but passive components, such as in TAKUTA and a capacitor, may be formed and semiconductor-integrated-circuit-ized.

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* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view of the SOI substrate in which the 1st operation gestalt of this invention is shown.

[Drawing 2] It is the sectional view showing the production process of the semiconductor integrated circuit using the conventional SOI substrate.

[Drawing 3] It is the sectional view showing the production process of the SOI substrate of drawing 1.

[Drawing 4] It is the sectional view showing the production process of the semiconductor integrated circuit using the SOI substrate of drawing 1.

[Drawing 5] It is the sectional view of the SOI substrate in which the 2nd operation gestalt of this invention is shown.

[Drawing 6] It is the sectional view showing the production process of the SOI substrate of drawing 5.

[Drawing 7] It is the top view of the SOI substrate in which the 3rd operation gestalt of this invention is shown.

[Description of Notations]

11 41 Substrate substrate

12 42 Dielectric film

32, 33, 43, 44 Silicon layer field

20 50 The 1st silicon substrate

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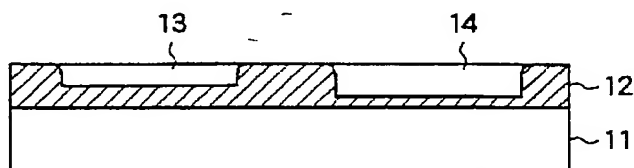
(54) 【発明の名称】 半導体基板、半導体集積回路及び半導体基板の製造方法

(57) 【要約】

【課題】 S O I 基板において、完全空乏型 M O S トランジスタと部分空乏型 M O S トランジスタのゲートを精度よく形成する。

【解決手段】 S O I 基板は、下地基板 1 1 と、下地基板 1 1 上に積層された誘電体膜 1 2 とを有しているが、該誘電体膜 1 2 の上には異なる 2 種類の膜厚のシリコン層領域 1 3、1 4 が形成されている。シリコン層領域 1 3、1 4 の表面高さは同じになっている。そのため、シリコン層領域 1 3、1 4 上に形成されるトランジスタのゲート電極の高さを揃えることができ、塗布するレジスト厚さが均一化でき、ゲート長を精度よく形成できる。

11 : 下地基板
12 : 誘電体膜
13, 14 : シリコン層領域



本発明の第 1 の実施形態の SOI 基板

【特許請求の範囲】

【請求項1】 誘電体膜によって下地基板から絶縁されたシリコン層を有する半導体基板において、前記シリコン層は異なる少なくとも2種類以上の膜厚を持つ複数のシリコン層領域を形成し、該各シリコン層領域間は電氣的に絶縁すると共に該各シリコン層領域の表面は同じ高さにしたことを特徴とする半導体基板。

【請求項2】 前記各シリコン層領域間は、前記誘電体を充填することで絶縁したことを特徴とする請求項1記載の半導体基板。

【請求項3】 前記各シリコン層領域は、前記誘電体膜上に分離して形成したことを特徴とする請求項1記載の半導体基板。

【請求項4】 前記各シリコン層領域は、少なくとも2個以上の素子が形成可能な面積をそれぞれ有することを特徴とする請求項1、2または3記載の半導体基板。

【請求項5】 請求項1、2、3または4記載の半導体基板上における前記2種類以上の膜厚のシリコン層領域のうち、膜厚の薄いシリコン層領域には完全空乏型MOSトランジスタまたは該完全空乏型MOSトランジスタを用いた回路を形成し、前記2種類以上の膜厚のシリコン層領域のうち、膜厚の厚いシリコン層領域には部分空乏型MOSトランジスタまたは該部分空乏型MOSトランジスタを用いた回路を形成したことを特徴とする半導体集積回路。

【請求項6】 請求項1、2、3または4記載の半導体基板上における前記2種類以上の膜厚のシリコン層領域のうち、膜厚の薄いシリコン層領域にはMOSトランジスタまたは該MOSトランジスタを用いた回路を形成し、前記2種類以上の膜厚のシリコン層領域のうち、膜厚の厚いシリコン層領域にはバイポーラトランジスタまたは該バイポーラトランジスタを用いた回路を形成したことを特徴とする半導体集積回路。

【請求項7】 請求項1、2、3または4記載の半導体基板上における前記シリコン層領域には、パッシブ素子を形成したことを特徴とする半導体集積回路。

【請求項8】 請求項1、2または4記載の半導体基板を製造する半導体基板の製造方法において、第1のシリコン基板に少なくとも2回以上の選択酸化をすることにより、少なくとも3種類以上の膜厚の異なるシリコン酸化膜領域を該第1のシリコン基板の表面側に形成する工程と、前記第1のシリコン基板の表面側を平坦化し、前記各シリコン酸化膜領域におけるシリコン酸化膜の一部を残して除去する工程と、前記平坦化された前記第1のシリコン基板の表面側に前記下地基板となる第2のシリコン基板を貼合わせる工程と、前記第1のシリコン基板の一部を裏面側から除去する工

程とを、順に行うことを特徴とする半導体基板の製造方法。

【請求項9】 請求項1、3または4記載の半導体基板を製造する半導体基板の製造方法において、第1のシリコン基板の表面側に溝を形成すると共に、少なくとも1回以上の選択酸化をすることにより、少なくとも2種類以上の膜厚の異なるシリコン酸化層を形成する工程と、前記第1のシリコン基板の表面側を少なくとも一部の前記シリコン酸化膜層を残して平坦化する工程と、前記平坦化された前記第1のシリコン基板の表面側に前記下地基板となる第2のシリコン基板を貼合わせる工程と、前記第1のシリコン基板の一部を裏面側から除去する工程とを、順に行うことを特徴とする半導体基板の製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、半導体基板、半導体基板に形成される半導体集積回路及び該半導体基板の製造方法に関するものである。

【0002】

【従来の技術】絶縁基板または絶縁膜上に薄膜シリコン層を形成した半導体基板、つまり、SOI (Silicon On Insulator) 基板に形成されたCMOS (Complementary Metal Oxide Semiconductor) トランジスタは、ソース・ドレイン間の接合容量が小さく、ラッチアップを防止できる等の理由で、半導体集積回路の低消費電力化を進める上で、注目されている。SOI構造上に形成されるCMOSトランジスタには、完全空乏 (Fully Depleted) 型と部分空乏 (Partially Depleted) 型とがある。完全空乏型は、薄膜シリコン層が50nm程度以下と薄く、ソース領域及びドレイン領域に挟まれたボディ領域が常に空乏化されている。部分空乏型では、薄膜シリコン層が100nm以上と比較的厚く、ボディ領域の底部が空乏化されていない。完全空乏型MOSトランジスタは、急峻なサブスレッショルド特性が得られ、オフリーク電流を抑制しつつ閾値電圧を低くできるので、低消費電力化に有効であるが、同時に薄膜シリコン層が50nm程度以下と薄いので、ソース・ドレイン抵抗が高く、基板濃度を高く設定するために易動度が低下してトランジスタの駆動能力が低下する等の欠点がある。

【0003】これに対し、部分空乏型MOSトランジスタは、サブスレッショルド特性がバルク基板上のMOSトランジスタと同程度となり、低消費電力化の効果が完全空乏型程には大きくない。しかしながら、ボディ領域の電位を固定することにより、動作中にインパクトイオン化によって生じた空孔がボディ領域に蓄積し、ドレイン電流特性に歪みを生じさせる現象 (キンク現象) を抑えることができる。よって、低消費電力特性と動作時の

安定性を考慮し、同一 SOI 基板に完全空乏型 MOS トランジスタと部分空乏型 MOS トランジスタとを混載して半導体集積回路化することが提案されている。

【0004】図 2 (a) ~ (e) は、従来の SOI 基板を用いた半導体集積回路の製造工程を示す断面図である。従来、同一 SOI 基板に完全空乏型の MOS トランジスタと部分空乏型の MOS トランジスタとを形成するときには、図 2 (a) ~ (e) の工程を順に行う。まず、図 2 (a) の工程において、シリコン単結晶基板中に酸素イオンを注入して酸化する SIMOX (Separation by Implanted Oxygen) 法と呼ばれる方法、あるいは次の文献に示される貼合わせ法と呼ばれる方法により、シリコン基板 1 上にシリコン酸化膜層 2 を形成し、その上に約 200 nm 程度の薄膜シリコン層 (以下「SOI 層」という。) 3 を有する SOI 基板を形成する。文献：特開平 5-275663 号公報

【0005】図 2 (b) の工程において、SOI 基板上に図示しないシリコン酸化膜のバッファ層及びシリコン窒化膜層を形成し、ホトリソ工程を経てシリコン窒化膜及びシリコン酸化膜に開口部を形成した後、該シリコン窒化膜をマスクとして SOI 層 3 を選択的に酸化し、シリコン窒化膜及びシリコン酸化膜を除去する。これにより、SOI 層が例えば 70 nm に薄くなった領域 4 を形成する。図 2 (c) の工程において、SOI 層 3 を選択的にエッチングし、領域 4 以外の場所に、部分空乏型 MOS トランジスタを形成する領域 6 を形成すると共に、領域 4 を含む場所に完全空乏型 MOS トランジスタを形成する領域 5 を形成する。この図 2 (c) の工程の次に、CMOS トランジスタを形成する。なお、図 2

(d) 及び (e) では、N チャネル型 MOS トランジスタ (以下「NMOS」という。) を形成する場合を説明しているが、P チャネル型 MOS トランジスタ (以下「PMOS」という) を形成する場合も、不純物のタイプを代えるだけで同様の工程で形成できる。

【0006】図 2 (d) の工程において、MOS トランジスタの閾値電圧を制御するための P 型不純物を注入し、ゲート酸化膜 7 を領域 5、6 の SOI 層 3 上に積層し、その上にゲート電極となるポリシリコン 8 を形成する。さらに、SOI 層 3 の一部に高濃度 P 型不純物を注入し、部分空乏型 MOS トランジスタのソースとなる部分に P⁺ 領域 9 を生成する。図 2 (e) の工程において、N 型不純物を高濃度に注入し、ソース及びドレインとなる N⁺ 領域 10 を SOI 層 3 に形成する。このとき、P⁺ 領域 9 の一部には、N 型不純物を注入せず、注入しない部分は P⁺ 不純物領域のままとなり、N 型不純物を注入した P⁺ 領域 9 の底部は、P 型不純物領域になる。以上により、完全空乏型 MOS トランジスタと部分空乏型 MOS トランジスタとが形成される。この MOS トランジスタが形成された基板に層間絶縁膜を積層した後、ソース、ドレイン、ゲート及びボディコンタクト領

域にコンタクトホールを開口し、メタル配線を形成して半導体集積回路を製造する。

【0007】

【発明が解決しようとする課題】しかしながら、従来の SOI 基板に半導体集積回路を形成する製造方法では、次のような課題があった。完全空乏型 MOS トランジスタのゲート電極を形成する領域 4 が、凹状になっているので、ゲート電極となるポリシリコン 8 を形成するためにレジスト膜を塗布する際に、該レジスト膜厚が周辺より厚くなり、ゲート長寸法の制御が困難になりやすく、また、エッチングの際にゲート電極がくびれる等の問題を生じることがあった。さらに、完全空乏型 MOS トランジスタと部分空乏型 MOS トランジスタのゲート電極の高さが異なるので、両方のトランジスタのゲート長寸法を合わせることが困難であった。

【0008】

【課題を解決するための手段】前記課題を解決するために、第 1 の発明は、誘電体膜によって下地基板から絶縁されたシリコン層を有する SOI 基板において、次のような構成にしている。即ち、前記シリコン層は異なる少なくとも 2 種類以上の膜厚を持つ複数のシリコン層領域を形成し、該各シリコン層領域間は電氣的に絶縁すると共に該各シリコン層領域の表面は同じ高さになっている。第 2 の発明は、第 1 の発明の SOI 基板において、前記各シリコン層領域の間は、前記誘電体を充填することで絶縁している。第 3 の発明は、第 1 の発明の SOI 基板において、前記各シリコン層領域は、前記誘電体膜上に分離されて形成している。第 4 の発明は、第 1、第 2 または第 3 の発明の SOI 基板において、前記各シリコン層領域は、少なくとも 2 個以上の素子が形成可能な面積をそれぞれ有する構成にしている。

【0009】第 5 の発明は、半導体集積回路において、第 1 ~ 3 または第 4 の発明の SOI 基板上における前記 2 種類以上の膜厚のシリコン層領域のうちの膜厚の薄いシリコン層領域には、完全空乏型 MOS トランジスタまたは該完全空乏型 MOS トランジスタを用いた回路を形成し、前記 2 種類以上の膜厚のシリコン層領域のうちの膜厚の厚いシリコン層領域には、部分空乏型 MOS トランジスタまたは該部分空乏型 MOS トランジスタを用いた回路を形成している。第 6 の発明は、半導体集積回路において、第 1 ~ 3 または第 4 の発明の SOI 基板上における前記 2 種類以上の膜厚のシリコン層領域のうちの膜厚の薄いシリコン層領域には、MOS トランジスタまたは該 MOS トランジスタを用いた回路を形成し、前記 2 種類以上の膜厚のシリコン層領域のうちの膜厚の厚いシリコン層領域には、バイポーラトランジスタまたは該バイポーラトランジスタを用いた回路を形成している。

【0010】第 7 の発明は、半導体集積回路において、第 1 ~ 3 または第 4 の発明の SOI 基板上におけるシリコン層領域には、パッシブ素子を形成している。第 8 の発

明は、第1、2または第4の発明の半導体基板を製造する半導体基板の製造方法において、次のような方法を講じている。即ち、第1のシリコン基板に少なくとも2回以上の選択酸化をすることにより、膜厚の異なる少なくとも3種類以上のシリコン酸化膜領域を該第1のシリコン基板の表面側に形成する工程と、前記第1のシリコン基板の表面側を平坦化し、前記各シリコン酸化膜領域におけるシリコン酸化膜の一部を残して除去する工程と、前記平坦化された前記第1のシリコン基板の表面側に前記下地基板となる第2のシリコン基板を貼合わせる工程と、前記第1のシリコン基板の一部を裏面側から除去する工程とを、順に行うようにしている。

【0011】第9の発明は、請求項1、3または4記載の半導体基板を製造する半導体基板の製造方法において、第1のシリコン基板の表面側に溝を形成すると共に、少なくとも1回以上の選択酸化をすることにより、膜厚の異なる少なくとも2種類以上のシリコン酸化層を形成する工程と、前記第1のシリコン基板の表面側を少なくとも一部の前記シリコン酸化膜層を残して平坦化する工程と、前記平坦化された前記第1のシリコン基板の表面側に前記下地基板となる第2のシリコン基板を貼合わせる工程と、前記第1のシリコン基板の一部を裏面側から除去する工程とを、順に行うようにしている。

【0012】第1から第9の発明によれば、以上のようにS O I基板、半導体集積回路及びS O I基板の製造方法を構成したので、膜厚の異なるシリコン層領域が誘電体膜上に形成され、かつ、それらのシリコン層領域の表面の高さが同じである。そのため、S O I基板のシリコン領域上に形成するM O Sトランジスタのゲート電極の高さが揃うことになる。また、第4の発明によれば、各シリコン層領域は、少なくとも2個以上の素子が形成可能な面積をそれぞれ持つので、例えば膜厚の薄いシリコン層領域に、完全空乏型M O Sトランジスタを用いた回路を形成し、膜厚の厚いシリコン層領域に、部分空乏型M O Sトランジスタを用いた回路を形成することで、高速性及び低消費電力性を持つ回路と、安定性が求められる回路とが共通基板に混載される。

【0013】

【発明の実施の形態】第1の実施形態

図1は、本発明の第1の実施形態を示すS O I基板の断面図である。このS O I基板は、下地基板11と、該下地基板11上に積層された誘電体膜12とを有し、該誘電体膜12の上には異なる2種類の膜厚のシリコン層領域13、14が形成されている。シリコン層領域13、14の間は、誘電体膜12によって電氣的に分離されると共に、該シリコン層領域13、14の表面高さは、同じになっている。

【0014】図3(a)～(e)は、図1のS O I基板の製造工程を示す断面図である。図4(a)～(c)は、図1のS O I基板を用いた半導体集積回路の製造工

程を示す断面図である。図1のS O I基板を形成するには、図3(a)～(e)の工程を順に行う。最初の図3(a)の工程は、3層構造の第1のシリコン基板20を形成する工程であり、P型シリコン基板21の表面に約20 μ mの厚さの多孔質シリコン層22を形成して酸化した後、C V D (Chemical Vapor Deposition) 法により、約200nm厚の単結晶シリコン層23をエピタキシャル成長させる。

【0015】図3(a)の次の図3(b)の工程では、単結晶シリコン層23の表面にバッファ層となるシリコン酸化膜層24を積層すると共にシリコン窒化膜層25を形成した後、ホトリソ工程により該シリコン窒化膜層25の一部分26を開口する。そして、選択酸化を行い、部分26におけるシリコン酸化膜の膜厚を約50nmの厚さにする。図3(c)の工程において、シリコン窒化膜層25が残っている領域のうちの一部分27に対してホトリソ工程を行い該シリコン窒化膜層25の除去し、選択酸化を行い、部分26におけるシリコン酸化膜の膜厚を約200nmに成長させる共に、部分27におけるシリコン酸化膜の膜厚を例えば約150nmにする。

【0016】図3(d)の工程において、残ったシリコン窒化膜層25を除去した後、熱酸化を行うことにより、単結晶シリコン層23がすべて酸化されたシリコン酸化膜領域28と、単結晶シリコン層23を約50nm残して酸化されたシリコン酸化膜領域29と、単結晶シリコン層23を約100nm残して酸化されたシリコン酸化膜領域30とを形成する。

【0017】図3(e)の工程において、化学的機械研磨法等により、図3(d)の基板の酸化された表面を平坦に研磨する。表面が研磨された基板を、別途用意された第2のシリコン基板31に、該研磨面が接するように重ね合せ、熱処理を行って強固に貼合わせる。貼合わされた基板のシリコン基板31側をシリコン窒化膜で被覆し、硝酸とフッ酸の混合液を用いて基板20側の多孔質シリコン層22を残してエッチング除去する。さらに、硝酸とフッ酸と酢酸の混合液を用いてその多孔質シリコン層22も除去する。これらのエッチングでは、単結晶シリコン層23は除去されない。よって、基板31の上に、該基板31とはシリコン酸化膜領域29、30で電氣的に分離されたS O I層32、33が形成される。S O I層32、33の間は、シリコン酸化膜領域28で電氣的に分離されている。即ち、図1のS O I基板が形成されている。基板31が下地基板11となり、シリコン酸化膜領域28、29、30が誘電体層12となり、S O I層32、33が、膜厚が異なるシリコン層領域13、14となる。

【0018】図1のS O I基板を用いて例えばCMOSトランジスタを持つ半導体集積回路を製造する場合には、図4(a)～(c)の工程を順に行う。なお、図4

(a)～(c)では、NMOSを形成する場合を説明しているが、PMOSを形成する場合も、不純物のタイプを代えるだけで同様の工程で形成できる。まず、図4

(a)の工程において、MOSトランジスタの閾値電圧を制御するためにP型不純物を注入し、シリコン層領域13、14を構成するSOI層32、33及び露出した誘電体膜12の表面にゲート酸化膜34を積層し、該ゲート酸化膜34上にレジストを塗布した後、電子ビーム露光法によってレジストパターンを形成する。そして、レジストパターンをマスクとしたドライエッチングを行い、ゲート電極35を形成する。

【0019】図4(b)の工程において、主表面全面にシリコン酸化膜を形成し、異方性エッチングを行い、ゲート電極35の側壁にサイドウォール36を形成する。図4(c)の工程において、MOSトランジスタのソース領域とドレイン領域とに、N型不純物を注入してN⁺層37を形成した後、CVD法により、W(タンゲステン)膜38を基板の主表面に選択成長させる。さらに、W膜38が形成された基板の主表面に層間絶縁膜を堆積した後、ソース、ドレイン、ゲート及びボディコンタクト領域にコンタクトホールを開口して、メタル配線を行う。以上の図4(a)～(c)の一連の工程により、半導体集積回路のMOSトランジスタが形成され、膜厚の薄いSOI層32の上に形成されたMOSトランジスタが完全空乏型MOSトランジスタとなり、膜厚の厚いSOI層33の上に形成されたMOSトランジスタが部分空乏型MOSトランジスタになる。ここで、ボディコンタクト領域は図示していないが、膜厚の厚いSOI層32上に形成される部分空乏型MOSトランジスタの例えば紙面手前側にある、ゲート電極35のないボディ領域に形成される。つまり、完全空乏型MOSトランジスタと、ボディ領域にコンタクトを有する部分空乏型MOSトランジスタとが半導体集積回路に混載されたことになる。

【0020】以上のように、この第1の実施形態では、図3(a)～(e)の製造工程で、完全空乏型MOSトランジスタを形成するのに適した膜厚の薄いSOI層32と部分空乏型MOSトランジスタを形成するのに適した膜厚の厚いSOI層33とが誘電体膜12で分離されると共にその表面高さが平坦になったSOI基板を形成している。そのため、SOI基板を用いて半導体集積回路を製造すると、完全空乏型MOSトランジスタと部分空乏型MOSトランジスタのポリシリコンの高さが揃い、塗布するレジスト膜厚が一定となり、ゲート電極35の長さを精度良く均一に形成できる。よって、パタンのくびれ等のない良好な半導体集積回路の形成が可能になる。その上、同一基板上に、完全空乏型MOSトランジスタと部分空乏型MOSトランジスタとをほぼ同一の工程で形成できるので、低コスト化に優れると共に、生産性が向上する。さらに、SOI層31、32の膜厚

が、単結晶シリコンのエピタキシャル成長工程及び酸化工程等で決まるので、膜厚の制御が容易であると共にその均一性が優れている。

【0021】第2の実施形態

図5は、本発明の第2の実施形態を示すSOI基板の断面図である。このSOI基板は、下地基板41から誘電体膜42によって絶縁されたシリコン層を有する基板であって、該シリコン層は異なる少なくとも2種類以上の膜厚を持つシリコン層領域43、44を形成し、該各シリコン層領域43、44間は溝で電気的に絶縁されると共に該各シリコン領域43、44の表面は同じ高さになっている。

【0022】図6(a)～(d)は、図5のSOI基板の製造工程を示す断面図であり、この図6(a)～

(d)を参照しつつ、図5のSOI基板の製造方法を説明する。まず、図6(a)の工程は、3層構造の第1のシリコン基板50を形成する工程であり、P型シリコン基板51の表面に約10μmの厚さの多孔質シリコン層52を形成して酸化した後、CVD法により、約200nm厚の単結晶シリコン層53をエピタキシャル成長させる。

【0023】図6(a)の次の図6(b)の工程では、熱酸化によつて単結晶シリコン層53上にシリコン酸化膜54を形成し、さらに、該シリコン酸化膜54上にシリコン窒化膜55を形成する。続いて、ホトリソ工程により、シリコン窒化膜55及びシリコン酸化膜54を部分的に開口し、単結晶シリコン層53を多孔質シリコン層52に届くまでエッチングし、単結晶シリコン層53を溝56で分断した構造を形成する。図6(c)の工程において、ホトリソ工程によってシリコン窒化膜55を部分的に除去した後、選択酸化により、約300nm厚のシリコン酸化膜領域57を形成する。

【0024】図6(d)の工程において、化学的機械研磨法等により、シリコン窒化膜55がなくなるまで、研磨して表面を平坦化する。このとき、シリコン酸化膜領域57の一部は研磨されずに残る。表面が研磨された基板を、別途用意された第2のシリコン基板41に、該研磨面が接するように重ね合せ、熱処理を行って強固に貼合わせる。貼合わされた基板のシリコン基板41側をシリコン窒化膜で被覆し、硝酸とフッ酸の混合液を用いて基板50側の多孔質シリコン層52を残してエッチング除去する。さらに、硝酸とフッ酸と酢酸の混合液を用いてその多孔質シリコン層52も除去する。これらのエッチングでは、単結晶シリコン層53は除去されない。よって、基板41の上に、該基板41とはシリコン酸化膜54、57で電気的に分離されたSOI層58、59が形成される。SOI層58、59の間には、溝56があり、電気的に分離されている。即ち、図5のSOI基板が形成されている。シリコン酸化膜54、57が誘電体層42となり、SOI層58、59が、膜厚が異なるシ

リコン層領域43、44となる。

【0025】以上のように、この第2の実施形態では、図6(a)～(d)で、完全空乏型MOSトランジスタを形成するのに適した膜厚の薄いSOI層58と部分空乏型MOSトランジスタを形成するのに適した膜厚の厚いSOI層59とが溝56で分離されると共にその表面高さが平坦になったSOI基板を形成している。そのため、第1の実施形態と同様に、SOI基板を用いて半導体集積回路を製造すると、完全空乏型MOSトランジスタと部分空乏型MOSトランジスタのポリシリコンの高さが揃い、塗布するレジスト膜厚が一定となり、ゲート電極35の長さを精度良く均一に形成できる。よって、パタンのくびれ等のない良好な半導体集積回路の形成が可能になる。

【0026】第3の実施形態

図7は、本発明の第3の実施形態を示すSOI基板の平面図であり、第1の実施形態を示す図1中の要素と共通の要素には共通の符号が付されている。このSOI基板は、例えば第1の実施形態と同様の工程によって製造された基板であり、膜厚が約50nmのSOI層で形成されたシリコン層領域13と、膜厚が約100nmのSOI層で形成されたシリコン層領域14とを有している。シリコン層領域13とシリコン層領域14との間は、シリコン酸化膜層で形成された誘電体膜12で分離されている。シリコン層領域13及びシリコン層領域14は、それぞれ2個以上のMOSトランジスタが形成可能な面積をそれぞれ持っている。膜厚の薄いシリコン層領域13には、完全空乏型MOSトランジスタを用いたデジタル回路群を形成し、膜厚の厚いシリコン層領域14には、部分空乏型MOSトランジスタを用いたアナログ回路群を形成するようになっている。このようにすることで、アナログ回路群とデジタル回路群とを共通の基板に混載することが可能になっている。

【0027】以上のように、この第3の実施形態では、シリコン層領域13及びシリコン層領域14が、それぞれ2個以上のMOSトランジスタが形成可能な面積を持つSOI基板になっており、アナログ回路群とデジタル回路群とが混載可能になっている。そのため、完全空乏型MOSトランジスタを用いた、高速性及び低消費電力性に優れたデジタル回路群と、ボディコンタクトを有する部分空乏型MOSトランジスタを用いた、動作時の安定性が高いアナログ回路群とを、同様の工程で同時に製造できるようになる。よって、高性能のアナログ・デジタル混載回路を低コストで製造でき、生産性が高い。さらに、デジタル回路群とアナログ回路群とが誘電体膜12で分離されているため、デジタル回路群で発生する雑音が、アナログ回路群の領域に到達して該アナログ回路群の特性を劣化させることが防止できる。その上、デジタル回路群とアナログ回路群の規模がそれぞれほぼ同程度の製品について、予め、SOI層の膜厚

が異なる領域13、14を所定の場所に形成した基板を作成しておけば、回路設計から製造までの期間が大幅に短縮できる。

【0028】なお、本発明は、上記実施形態に限定されず種々の変形が可能である。その変形例としては、例えば次のようなものがある。

(1) 膜厚の薄いSOI層32、58に完全空乏型MOSトランジスタを形成し、膜厚の厚いSOI層33、59に部分空乏型MOSトランジスタを形成する構成にしたが、例えば、バイポーラトランジスタを該膜厚の厚いSOI層33、59に形成し、MOSトランジスタとバイポーラトランジスタとを混載した半導体集積回路を製造するようにしてもよい。

(2) SOI層32、33、58、59には、トランジスタばかりでなく、インタクタやキャパシタ等のパッシブ素子も形成して半導体集積回路化してもよい。

【0029】

【発明の効果】以上詳細に説明したように、第1～第9の発明によれば、膜厚の異なるシリコン層領域が誘電体膜上に形成され、かつ、それらのシリコン層領域の表面の高さが同じであるので、該シリコン層領域上に形成されるMOSトランジスタのゲート電極の高さが揃うことになり、該ゲート電極の長さが精度よく形成でき、パタンのくびれ等のない良好な半導体集積回路の形成が可能になる。その上、同一基板上に、完全空乏型MOSトランジスタと部分空乏型MOSトランジスタとをほぼ同一の工程で形成できるので、低コスト化に優れると共に、生産性が向上する。

【0030】そのうえ、第4の発明によれば、各シリコン層領域は、少なくとも2個以上の素子が形成可能な面積をそれぞれ持つので、例えば膜厚の薄いシリコン層領域に、完全空乏型MOSトランジスタを用いた回路を形成し、膜厚の厚いシリコン層領域に、部分空乏型MOSトランジスタを用いた回路を形成することで、高速性及び低消費電力性を持つデジタル回路と、安定性が求められるアナログ回路とが共通基板に混載にできる。

【図面の簡単な説明】

【図1】本発明の第1の実施形態を示すSOI基板の断面図である。

【図2】従来のSOI基板を用いた半導体集積回路の製造工程を示す断面図である。

【図3】図1のSOI基板の製造工程を示す断面図である。

【図4】図1のSOI基板を用いた半導体集積回路の製造工程を示す断面図である。

【図5】本発明の第2の実施形態を示すSOI基板の断面図である。

【図6】図5のSOI基板の製造工程を示す断面図である。

【図7】本発明の第3の実施形態を示すSOI基板の平

面図である。

【符号の説明】

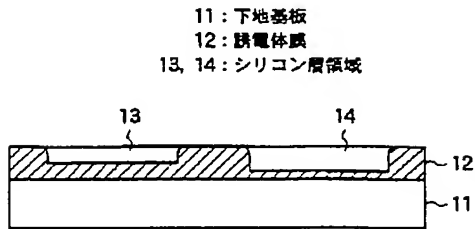
11, 41 下地基板

12, 42 誘電体膜

32, 33, 43, 44 シリコン層領域

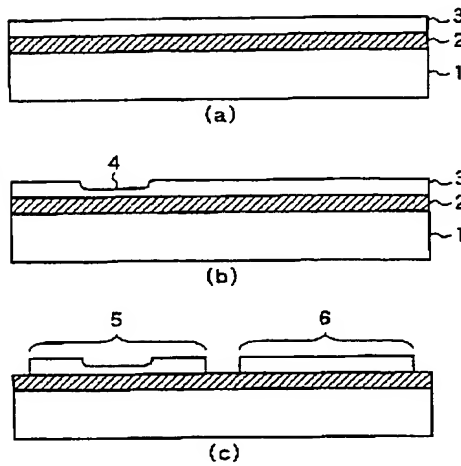
20, 50 第1のシリコン基板

【図1】

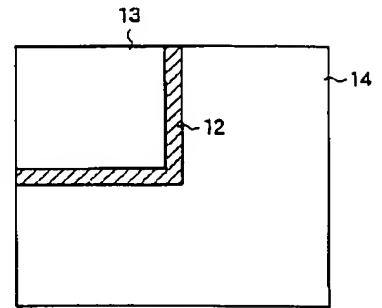


本発明の第1の実施形態のSOI基板

【図2】



【図7】



本発明の第3の実施形態のSOI基板

【図4】

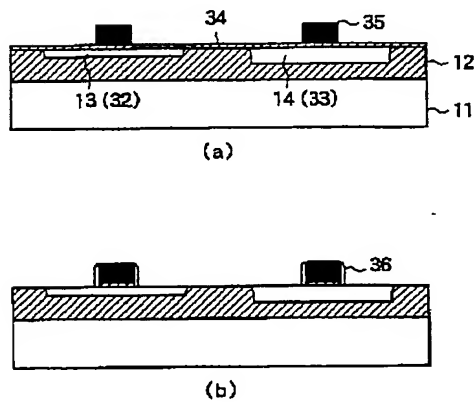
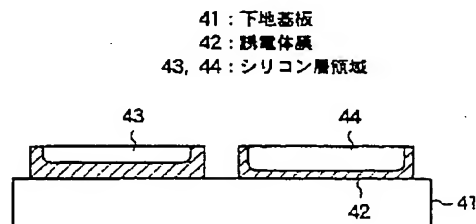


図1を用いた半導体集積回路の製造工程

【図5】



本発明の第2の実施形態のSOI基板

従来の半導体集積回路の製造工程

41: 下地基板

42: 誘電体膜

43, 44: シリコン層領域

【図3】

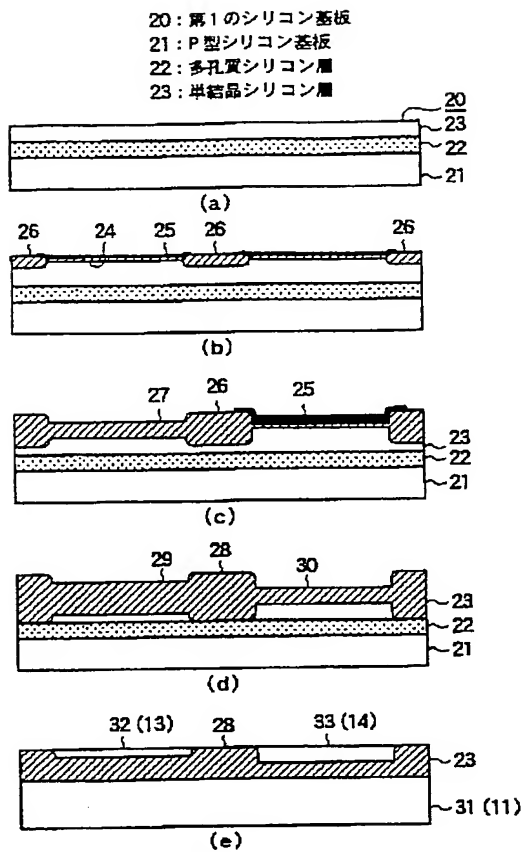


図1のSOI基板の製造工程

【図6】

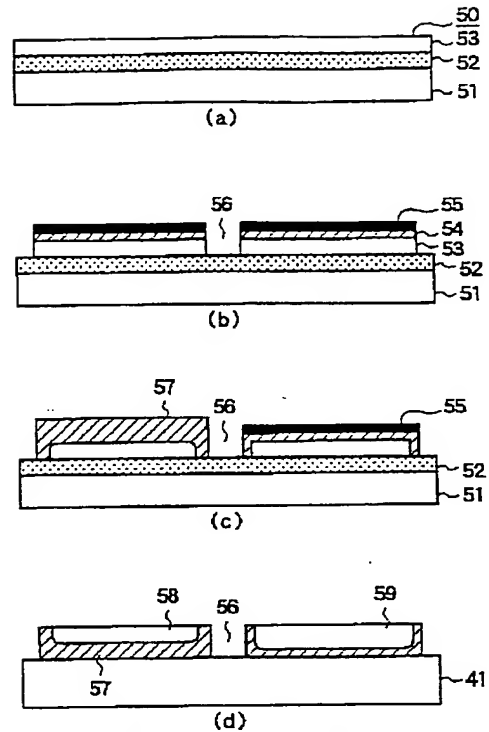


図5のSOI基板の製造工程

フロントページの続き

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